REMARKS

(A) Claims 1, 5, 7, 8, 14 & 17 objections:

Please find the amended claims in compliance with the examiner's request. Withdrawal of the objections to the claims is respectfully requested.

(B) 35 USC 102 Rejections:

A Section 102 rejection requires that each and every element recited in the claims be present in the reference. However, as shown below, Duong fails to show all claim elements.

In rejecting claim 1, on page 3, the examiner stated: *"a second selectable fabricating option (e.g. antifuse; col. 4, lines 48+) comprising hard-wired circuit in lieu of said user configurable memory circuit, wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options (it is inherent since (e.g.) the path from 120 to any of line 12, 18, 16, or 14 will not be changed, only the memory cells such as 210b will be changed; therefore neither functionality nor performance will be changed)"*.

The Applicant believes that the Examiner may have misinterpreted Fig-2 in Duong. Fig-2 combines block-diagrams (e.g. 10, 20, 30, 40, 236, 110, 232, 234, 210b, 220b, 230b, 240b) and circuit elements (e.g. 210a, 220a, 230a, 240a, 120) to show Duong invention. The circuit elements inside above listed blocks are not shown. However, the Applicant discloses such circuits in Applicant's Fig-3, 4 & 5. The SRAM circuit in Fig-3A (potential SRAM circuit for 210b in Duong) and anti-fuse circuit in Fig-4B (potential anti-fuse circuit for 210b in Duong) shown by the Applicant are duplicated below. Such circuits can generate S_0 control signal to activate the pass-gate 210a. These memory circuits also comprise transistors similar to 210a, 220a, 230a, 240a shown in Duong Fig-2.

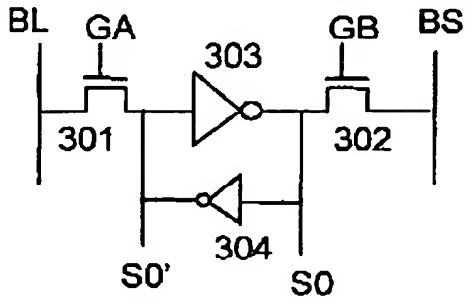

Fig-3A

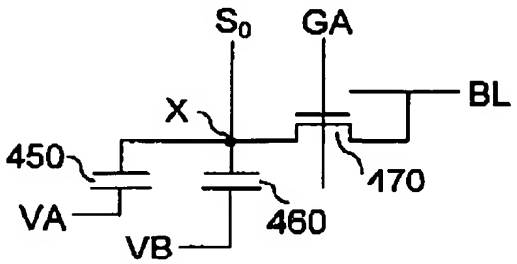

Fig-4B

Assume a Duong Fig-2 construction with SRAM elements. The most common SRAM circuit in Fig-3A comprises 6 transistors; four NMOS transistors exactly analogous to 210a-240a as in Duong Fig-2, two PMOS transistors (inside inverters 303 & 304) exactly analogous to PMOS transistors inside buffer 120 in Duong Fig-2. To complete functionality of SRAM memory, they are interconnected by metal wires; most notable are word-lines GA & GB, and bit-lines BL & BS. Data must be written into these SRAM cells; thus decoding circuits, drivers, registers and other supporting circuitry are provided within the IC to support an SRAM based Fig-2 device. One familiar in the art is assumed to know these basics by Duong.

Assume a Duong Fig-2 construction with anti-fuse pull-up and pull-down elements. The Applicant's anti-fuse construction in Fig-4B is such a choice. Capacitors 450 & 460 are the pull-up, pull-down choices. Fig-4B has one NMOS transistor 470, one bit-line BL, one word-line GA and two capacitors 450 & 460. The NMOS 470 is a special high-voltage (HV) transistor unlike the NMOS 210a-240a in Duong Fig-2. The capacitor elements 450 & 460 are different to transistor elements in SRAM, and a different process (from an SRAM process) capable of producing capacitors and HV transistors is required. The anti-fuse capacitors can be between two metals, between two poly plates, or between poly & diffusion. It is well known in the art that high voltage (HV) transistors have special layout geometries to support high voltages. Even the gate oxide thickness for a HV transistor is thicker than a typical NMOS 210a in Duong Fig-2. Special junctions with deep implant profiles are needed to sustain high voltages. Additional thermal cycles are required in the process to construct the special gate oxides and deep junctions. The extra thermal cycles alter NMOS 210a transistor profiles. Anti-fuse based Fig-2 device is not a hard-wired device, it is a configurable device. Data must be programmed/burned to these anti-fuse cells; thus decoding circuits, drivers, registers and other supporting circuitry is provided within the IC to support anti-fuses. Anti-fuse elements require a high voltage across the capacitor to pop the dielectric. This is how an anti-fuse element is programmed, and further described in Attachment-A (page 112, sec. 3.2.1). Hence high-voltage pumps and high voltage decoding circuits, totally different to those in SRAM circuits are needed. As stated by Duong, one familiar in the art is expected to know these basic differences.

SRAM data is volatile – when powered down, data is lost. Additional circuitry within the IC determines a power down event and ensures new data is loaded correctly. Anti-fuse data is non-volatile, and no such power-up data loading circuitry is required. In Duang disclosure, one

with ordinary skill is expected to know these subtle differences between SRAM and anti-fuses when reading col 4 lines 48+. These differences were cited by the Applicant in Ref-2 in the IDS form by ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA. Key pages 110-117 containing SRAM & anti-fuses are provided as Attachment-A in this response for the examiner's convenience.

A device top view fabricated with the block/circuit diagram in Duong Fig-2 has no resemblance to Fig-2. This is determined by a layout data base that comprises mask data. The masks include silicon diffusion geometries, gate poly geometries, contacts to diffusion / poly, metal geometries and vias between metal. Such a layout is not shown by Duong. In such a layout, all memory 210b and pass-gate 210a transistors are inter-dispersed over the Silicon surface. The total Silicon area needed is determined by every single transistor that resides on the surface. For example, for 1 Million SRAM cells, 6 Million transistors reside on Si surface. For 1 Million anti-fuse cells, 1 Million high voltage transistors reside on Si surface. (If poly-to-diffusion capacitors are utilized, 2 Million such capacitors also reside on Si surface, if metal-to-metal capacitors are utilized they may not occupy Si surface area). Coupled pairs such as 210a & 210b are distributed across the silicon foot-print. It is clear that 6 Million NMOS/PMOS transistors for an SRAM construction and 1 Million HV transistors for anti-fuse construction cannot have an identical Silicon foot-print. It is well known to one familiar in the art that Si patterns and wire patterns significantly change between SRAM and anti-fuse constructions of the same device, even if transistors such as 210a in Fig-2 is unchanged. Even the device size (also known as die size) is different. These differences are further exacerbated by the different supporting circuitry needed for each memory type; those circuit elements further inter-dispersed within the IC. Just as the Si diffusion mask (also known as active area mask) is different, so is every other mask between SRAM and anti-fuse constructions.

What is stated thus far is common knowledge to one familiar in the art of design and manufacture of ICs. Duong prior art cited by the examiner impliedly assumes that this knowledge resides in the reader. No SRAM or anti-fuse memory is provided, no programming is discussed, no supporting circuits for memory are disclosed, no construction of ICs is shown, and no layout information is provided. One who has fabricated SRAM and anti-fuse based products, also know that even NMOS transistor 210a in Duong Fig-2 will alter between SRAM and anti-fuse constructions due to HV related "extra thermal processing" (Attachment-A, p116, last para).

The applicant respectfully submits the following two traversals to the claim 1 rejection:

1) Anti-fuse circuit is not a hard-wire circuit. Anti-fuse circuit is another user-configurable circuit. In Attachment-A (p111, sec 3.2) anti-fuse is clearly listed under programming technologies. The Applicant provided an Anti-fuse circuit under configurable technology in the current application. Duong mentions such in col. 4 line 52. Duong does not show detailed elements of an anti-fuse circuit, while the applicant has done so in Applicant's Fig-4A (described on page 19 line 20 – page 20 line 15). How the user configures each element is fully described by the Applicant and in Attachment-A (page 112, sec. 3.2.1). Without programming, an anti-fuse circuit is non-functional, while a hard-wire circuit is always fully functional.

2) Performance is completely different between SRAM and anti-fuse construction options. It is not inherent that the path 120 to any of line 12, 18, 16, or 14 will not be changed. In Duong Fig-2, path from 120 to any line 12 is a layout characteristic, and not a block-diagram characteristic as the examiner may have interpreted. If memory cells such as 210b (and programming circuitry to support memory cells) change from SRAM to anti-fuses, the entire Silicon surface and wire patterns change, even if transistor 210a dimensions within Silicon layer is unchanged. Transistor 210a characteristic will actually change in anti-fuse processing due to extra high temperature processing steps. In a physical layout, the timing parameter depends on gate delay components and RC delay components. Gate delays depend on gate capacitance including Miller effect and junction capacitance. If doping profiles alter, gate delays will change. RC delays depend on wire length, wire resistance, current strength, repeaters within wire segments and neighboring wires. In Duong Fig-2, consider the timing delay between node 16 and node 18. The physical distance between the two nodes depend on circuit elements the signal traverses, and the supporting elements to program the path, and how these elements are physically located. The small circuit in Fig-2 without memory is ~ 20 transistors. It has 13 memory elements: if SRAM it is 78 (52 NMOS + 26 PMOS) transistors, if anti-fuse it is 13 HV NMOS + 26 Capacitors. The memory related elements far exceed the fixed elements, and totally dominate how the elements are arranged on the Silicon surface. The distances clearly change. The small circuit is under 15 System Gates; so in a typical IC of ~ 500,000 to 1,000,000 system gates, these node-to-node distances change significantly between SRAM and anti-fuse constructions.

In rejecting claim 4, on page 3, the examiner stated: "*Duong discloses, in Figs. 2-5, an input, said input received at an input pad (inherent input pad in IC: see col. 1, lines 12+); and*

an output, said output generated at an output-pad (inherent input pad in IC; see col. 1, lines 12+); and an input to output signal propagation delay, said delay substantially identical (path with RAM and path with ROM will be identical when they both have buffered mode; see col. 4, lines 10+, col. 2, lines 6+) between said first and said second selectable fabrication options (col. 4, lines 48+)".

The applicant respectfully submits the following added traversal to the rejection:

1) The input pad to output pad signal propagation delay comprises a plurality of gate delay and RC delay components encountered in that path. Specifically, the RC delay components depend on node-to-node distances and metal construction, which is determined by the configuration memory choice. Fig-2 does not provide any information on signal timing, and the Applicant has described how such signal delays depend on circuit layout impacted by memory choice.

In rejecting claim 5, on page 3, the examiner stated: "*wherein said hard-wire circuit comprises at least one custom mask (such as anitifuse pull-up and pull-down; col. 4, lines 48+), said at least one mask facilitating: a power-bus (pull-up to power supply to turn on the NMOS device; see col. 1, lines 50+, col. 5, lines 20+) connection to replace a logic one in said configurable memory circuit; and a ground-bus (pull-down to ground to turn off the NMOS device; see col. 1, lines 50+, col. 5, lines 20+) connection to replace a logic zero in said configurable memory circuit.*"

The applicant respectfully submits the following added traversal to the rejection:

1) In Duong, every single mask in an anti-fuse memory option is different from the SRAM memory option. This is caused by the "new" capacitor elements and "high-voltage" requirements to build anti-fuse elements. Even the process to fabricate an anti-fuse element is different from the process to fabricate SRAM elements. Anti-fuses do not provide a hard-wire circuit. Many masks are needed to build anti-fuse configuration circuits. After construction, anti-fuse devices are non-functional. In the anti-fuse construction, there is no custom mask facilitating a power bus connection, and there is no custom mask facilitating a ground bus connection. Anti-fuses must be programmed, in conjunction with other circuit elements, either to couple logic "1" or logic "0".

In rejecting claim 8, on page 4, the examiner stated: "*a programmable logic device (PLD) (col. 1, lines 12+) comprising: two selectable memory construction options (col. 4, lines 48+) to control logic circuits (210a, 220a, 230a, 240a), wherein: a first selectable option comprises a random access memory (RAM) construction (155; col. 4, lines 48+); and a second*

selectable option comprises a hard-wire read only memory (ROM) construction (155; col. 4, lines 48+); wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options (since pass transistors 210a, 220a, 230a, 240a will not be changed, only memory can be changed; col. 4, lines 48+)."

The applicant respectfully submits the following two traversals to the rejection:

1) Anti-fuse circuit is not a hard-wire ROM circuit. Anti-fuse circuit is a user-configurable ROM circuit. It is common knowledge to one familiar in the art that a hard-wire ROM circuit requires no end-of-line programming. In anti-fuse circuits, end-of-line programming is needed. In Attachment-A (page 111), anti-fuse is listed under programming technologies. How the user configures each anti-fuse element is fully described by the Applicant and in Attachment-A.

2) Logic circuits are fabricated with completely different masking patterns between SRAM and anti-fuse memory options for Duong device in Fig-2. The examiners assertion "since pass transistors 210a, 220a, 230a, 240a will not be changed, only memory can be changed; col. 4, lines 48+" is not correct. As the Applicant presented earlier, all diffusion geometries (memory, logic, transistors, capacitors, diodes) are folded into a common diffusion masking pattern. All gate poly geometries (memory, logic, transistors, capacitors, resistors) are folded into a gate poly pattern, etc. When transistors change between SRAM and anti-fuse memory options, these patterns also change. Pass transistors 210a, 220a, 230a, 240a will not be changed is not a sufficient criterion to ensure common masking pattern.

In rejecting claim 10, on page 4, the examiner stated: "*Duong discloses, in Figs. 2-5, wherein said second selectable option comprises mapping one of said first selectable option RAM bit patterns to a hard-wire ROM pattern (col. 4, lines 48+).*"

The applicant respectfully submits the following added traversal to the rejection:

1) Anti-fuse circuit is not a hard-wire ROM circuit. Anti-fuse circuit is a user-configurable ROM circuit. Hence equivalent RAM data must be programmed into anti-fuses. How the user configures each anti-fuse element is fully described by the Applicant and in Attachment-A. Hard-wire option is not equivalent to anti-fuses.

In rejecting claim 11, on page 5, the examiner stated: "*Duong discloses, in Figs. 2-5, an input, said input received at an input pad (inherent input pad in IC; see col. 1, lines 12+); and an output, said output generated at an output-pad (inherent input pad in IC; see col. 1, lines 12+); and an input to output signal propagation delay, said delay substantially identical (path*

with RAM and path with ROM will be identical when they both have buffered mode; see col. 4, lines 10+, col. 2, lines 6+) between said first and said second selectable fabrication options (col. 4, lines 48+)."

The applicant respectfully submits the following added traversal to the rejection:

1) The input pad to output pad signal propagation delay comprises a plurality of gate delay and RC delay components encountered in that path. Specifically, the RC delay components depend on node-to-node distances and metal construction, which is determined by the configuration memory choice. Fig-2 does not provide any information on signal timing, and the Applicant has described how such signal delays depend on memory circuitry choice.

In rejecting claim 16, on page 5, the examiner stated: "*wherein said programmable means in said second selectable option comprises hard-wiring a ROM bit (such as antifuse pull-up and antifuse pull-down. col. 4, lines 48+). said ROM bit providing: a hard-wire to power-bus (pull-up to power supply to turn on the NMOS device; see col. 1, lines 50+, col. 5, lines 20+) to connect said two nodes; and a hard-wire to ground-bus (pull-down to ground to turn off the NMOS device; see col. 1, lines 50+. col. 5. lines 20+) to disconnect said two nodes.*"

The applicant respectfully submits the following added traversal to the rejection:

1) Anti-fuses are different from hard-wire ROM bits. They provide programmable (or configurable) ROM bits that are customized after fabrication, in the field, prior to use. Hard-wired ROM bits are defined during fabrication. Anti-fuses couple to power or ground buses after they are programmed by selectively shorting dielectrics. Any memory option can provide a similar outcome. They do not provide hard-wire connections to power-bus or ground-bus, which is a hard-wire ROM. It is not clear to the Applicant how the examiner concluded the above from Duong col. 1 lines 50+ and col. 5 lines 20+.

Duong col 1 lines 50+: "*To couple line 16 with line 12, memory cell 10b is programmed such that transistor 10a conducts. If transistor 10a is an NMOS device, then memory 10b is programmed with a "1" to turn on. If transistor 10a is a PMOS device, then memory 10b is programmed with a "0" to turn on.*" Duong does not mention of a hard-wire to power or ground. It simply says that memory element must output a logic signal at a logic one or logic zero level. It is not even said that logic zero is ground voltage and logic one is at power voltage. Logic zero and logic one can be any two voltage levels that can be distinctly identified between a zero and one; in certain memory applications this difference is only 0.2 volts. It is well known that voltage

level (V_{cc}-V_{tN}) is an adequate "1" for NMOS, and voltage level "V_{ss}+V_{tP}" is an adequate "0" for PMOS. Such levels are often used in FPGA's.

Duong col. 5, lines 20+: "*The memory cells of switch block 155 can be SRAM, EPROM, EEPROM, flash memory, antifuse pull-up or pull-down, or composed of a number of other well known programmable memory cells. Like many FPGA devices, a number of well known mechanisms (including PROM device or antifuse programming method) can be used to program memory cells to configure switch box 155 of the present invention. Memory cells 210b, 220b, 230b, 240b, 232, 234, and 236, as well as memory cells 10b, 20b, 30b, 40b, 50b, 60b (Fig-1) are programmed during the initialization operation to configure box 155 of the present invention. The method and mechanisms to perform the required programming for each switch box of an FPGA or similar circuits are well known and therefore are not discussed.*" There is no mention of a hard-wire to power or ground. *Antifuse pull-up* does not mean there is a hard-wire to power-bus. It means there is a programmable antifuse element that provides coupling capability to an adequately high voltage level. That voltage level could be V_{cc} or (V_{cc}-V_{tN}) as both provide adequate logic "1" levels. In the anti-fuse construction, there is no custom mask facilitating a power bus connection or a ground bus connection. Anti-fuses must be programmed, in conjunction with other circuit elements, either to couple logic "1" or logic "0".

In rejecting claims 17-20, on page 6, the examiner stated: "*Claims 17-20 are essentially same as claims 1-16 as discussed above and are rejected similarly*".

The applicant respectfully submits the following two traversals to the rejection:

1) Duong does not demonstrate "a second selectable option comprising a hard-wire read only memory (ROM) construction". In the examiners second choice of antifuse circuits, there is no hard-wired ROM construction. It is a programmable read-only memory (PROM) construction.

2) Duong does not teach "the pass-gate logic element construction comprises one or more masking patterns that are invariant to the memory construction options". Duong pass-gates 210a, 220a, 230a, 240a, 10a, 20a, 30a, 40a are constructed with the transistors/capacitors in memory 210b, 220b, 230b, 240b, 10b, 20b, 30b, 40b. All masking patterns change for different memory options. Therefore, antifuse and SRAM do not have invariant masking patterns.

In the Response to Arguments on pages 6-7, the examiner stated: "*Also, it can be interpreted that this same IC of Duong is comprised of a second selectable fabrication option with a hard-wired circuit such as ROM or antifuse in lieu of said memory circuit. .... This means*

that no components on the path from one point to the other (e.g. from output 120 to any line of 12, 18, 16, or 14 having pass gates 210a, 220a, 230a, and 240a in between) will be changed. Only the programmable memory cells can be changed. Consequently, there will be no time difference or delay on the same paths for the two different options. Therefore, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options and the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction option as set forth in the claims" This statement has three basic misinterpretations that led to the rejection. All three misinterpretations fall under "common knowledge of one familiar in the art" as stated by Duong in col. 5 line 60.

1) Hard-wired circuit: Anti-fuse is not a hard-wired ROM. It is a Programmable ROM (PROM) that has to be configured by the user. The Applicant states that very distinctly on page 19 lines 20+, and Duong states that in col. 4 line 52. It is unclear to the Applicant why the examiner chose to consider antifuse as a hard-wire ROM. It is well known in the art that antifuse falls under user programmable technology (see Attachment-A, page 111, sec. 3.2).

2) Time difference (identical timing): "No components changed in the timing path" is necessary, but not sufficient to ensure no timing difference. The entire layout of the timing path must also not change. This includes transistors, wires, distances, neighboring capacitances, resistances, node positions, etc. Applicant's claims do not distinguish one specific timing path. Therefore every possible timing path in the device must not change. Thus the entire device layout must not change. Clearly, the entire device layout has to change between SRAM and anti-fuses even if only the memory choice is altered. In Fig-2 (which represents 0.001% of a full IC chip) there are more memory related transistors (78) that change compared to transistors (20) that do not change. It is well known in the art that block-diagrams do not provide timing characteristics, and layout information and SPICE extractions are needed to do so. It is well known in the art that logic process (for SRAM) and HV process (for anti-fuses) are vastly different. As a result, even NMOS transistor parameters are different between the two processes.

3) Common masking patterns: "No components changed in the timing path" is necessary, but not sufficient to ensure that common masking patterns are utilized. Masking pattern is not a block-diagram characteristic, it is a layout characteristic that very much depends on memory, logic, diffusion, poly, contact, metal-1, via, metal-2, and every other component. Even the basic

transistors are different between SRAM and anti-fuses. Clearly, the entire device layout must change between SRAM and anti-fuses even if only the memory choice is altered. It is well known in the art that logic process (for SRAM) and HV process (for anti-fuses) are vastly different.

The applicant believes that each of the independent claims (Claim 1, 8 & 17) were rejected due to misinterpretation of Duong teaching by the examiner. It is clear to one familiar in the art that: (i) anti-fuse circuit is not a hard-wire circuit; (ii) timing characteristics of an IC is not determined by a block diagram, and memory elements cannot be replaced from SRAM to anti-fuses without impacting the layout, fabrication process, and timing; and (iii) masking pattern is not a block-diagram characteristics, and memory elements cannot be replaced from SRAM to anti-fuses without impacting the layout. The applicant believes that the independent claims and those dependent thereupon (Claims 1-20) are not anticipated by Duong. Withdrawal of the rejections of claims 1-20 is respectfully requested.

CONCLUSION

Applicant believes that the above discussion is fully responsive to all grounds of objections and rejections set forth in the Office Action.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868, or cell phone (408) 431-5367.

Respectfully submitted,

Raminda U. Madurawe

Raminda U. Madurawe
Applicant